R18 Regulation *Subject code:* 2P5DB

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech V Semester Regular Examinations, February 2021

VLSI DESIGN

(Electronics and Communication Engineering)

Maximum Marks: 70 Date:19.02.2021 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks **(10x2M=20 Marks)**

1 What are the advantages of BiCMOS.
2 Define Figure of Merit.
3 List the steps in VLSI Design flow.
4 Sketch the CMOS 2 input NOR gate.
5 Express Propagation delay in a logic gate.
6 Define Fan In and Fan Out.
7 Draw the diagram of Zero cross detector.
8 Compare SRAM and DRAM.
9 List the advantages of CPLD.
10 Write Fault models in CMOS Testing.

Part-B

Answer All the following questions. **(10M X 5=50Marks)**

11 Explain NMOS fabrication steps with neat diagrams. (10M)

OR

12 a) Analyze CMOS Inverter. (5M)
b) Analyze BiCMOS Inverter. (5M)

13 Explain Lambda based Design Rules. (10M)

OR

14 a) Sketch the CMOS Transistor Layout for Y=(A+BC)' and Explain. (5M)
b) Sketch the nMos Inverter Layout and Explain. (5M)

15 a) Design a CMOS NAND Gate using Gate level design. (5M)
b) Write notes on Switch Logic and Time Delays. (5M)

OR

16 a) Design a nMOS NOR Gate using Gate level design. (5M)
b) Explain about Capacitive loads. (5M)

17 a) Design a Full Adder using Data Path Subsystem. (5M)
b) Explain about Parity generator. (5M)

OR

18 Explain read and write operations of 6T SRAM cell. (10M)

19 a) Explain the design of PLA with an example. (5M)
b) Write notes on need for Testing. (5M)

OR

20 a) What are the parameters influencing low power design? (5M)
b) Explain the Chip level Test Techniques. (5M)